REMARKS

Applicant thanks the Examiner for initialing the references listed on the PTO-1449 form submitted with the Information Disclosure Statement filed on January 22, 2002, thereby confirming that the listed references have been considered.

Applicant requests that the Examiner consider the references listed on the PTO-1449 forms submitted with the Information Disclosure Statement filed on December 30, 1999 and initial same, thereby confirming that the listed references have been considered.

Applicant herein amends the specification to remove the typographical errors pointed out by the Examiner. No new matter has been added. Entry of the amendments to the specification is respectfully requested.

Claims 1-15 and 17-30 have been examined on their merits.

Claim 16 remains withdrawn from consideration.

The Examiner objects to claims 2-15, 19-24, 29 and 30 as being dependent upon a rejected base claim. Applicant thanks the Examiner for indicating that 2-15, 19-24, 29 and 30 would be allowed if rewritten in independent form. However, instead of rewriting 2-15, 19-24, 29 and 30 in independent form, Applicant respectfully traverses the prior art rejections for the reasons set forth below.

Applicant herein amends claims 1, 4, 17 and 20. The amendments to claims 1, 4, 17 and 20 do not add any new matter. Entry and consideration of the amendments to claims 1, 4, 17 and 20 is respectfully requested.

Claims 1-30 are all the claims pending in the application.

1. Claims 1-15 and 17-30 stand rejected under 35 U.S.C. § 112, second paragraph as allegedly being indefinite.

Applicant herein amends claim 1 to add the phrase "second conductivity type" and to delete the phrase "other conductivity type."

The Examiner asserts that there is insufficient antecedent basis for the phrase "other of said emitter region or said collector region" recited in claim 1. As is well known in the art, a bipolar transistor comprises an emitter, a base and a collector. An earlier recitation in claim 1 recites the base of the bipolar transistor. Next, claim 1 recites that a "second impurity region is one of an emitter region or a collector region of said bipolar transistor." The second impurity region forms either the collector region or the emitter region of the bipolar transistor; it does not form both regions simultaneously. Finally, claim 1 recites a "third impurity region is the other of said emitter region or said collector region of said bipolar transistor", which plainly means that if the second impurity region is the collector region, then the third impurity region is the emitter region for the bipolar transistor. Applicant believes these recitations of claim 1 are not indefinite under 35 U.S.C. § 112, sixth paragraph, and Applicant notes that the Examiner did not reject a similar recitation of emitter and collector regions in claim 17.

Applicant herein amends claim 17 to add the phrase "in one of said active areas" and to delete the phrase "in said active area."

Applicant herein amends claim 20 to properly depend from claim 19, instead of claim 18.

Applicant believes that the amendments to claims 1, 17 and 20 have overcome the Examiner's rejection, and requests that the Examiner withdraw the § 112, sixth paragraph rejection of claims 1-15 and 17-30.

2. Claims 1, 17, 18 and 25-28 stand rejected under 35 U.S.C. § 102(e) as allegedly being anticipated by Porter et al. (U.S. Patent No. 6,355,508). Applicant traverses the rejection of claims 1, 17, 18 and 25-28 at least for the reasons set forth below.

To support a conclusion that a claimed invention lacks novelty under 35 U.S.C. § 102, a single source must teach all of the elements of a claim. *Hybritech Inc. v. Monoclonal Antibodies, Inc.*, 802 F.2d 1367, 1379 (Fed. Cir. 1986). A claim is anticipated only if each and every element as set forth in the claim is found either expressly or inherently in a single prior art reference. *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631 (Fed. Cir. 1987). A single source must disclose all of the claimed elements arranged as in the claim. *Richardson v. Suzuki Motor Co.*, 868 F.2d 1226, 1236 (Fed. Cir. 1989). Rejections under 35 U.S.C. § 102 are proper only when the claimed subject matter is identically disclosed or described in the prior art. Thus, the cited reference must clearly and unequivocally disclose every element and limitation of the claimed invention.

With respect to independent claims 1 and 17, Porter et al. fail to teach or suggest at least a third impurity region, which comprises one of an emitter region or a collector region of a bipolar transistor, that is located in a region disposed away from the active areas of a semiconductor device. The Examiner relies upon Figure 1 of Porter et al. to support the anticipation rejection of claim 1. The Examiner argues that the n-type impurity region (12) illustrated in Figure 1 of Porter et al. is

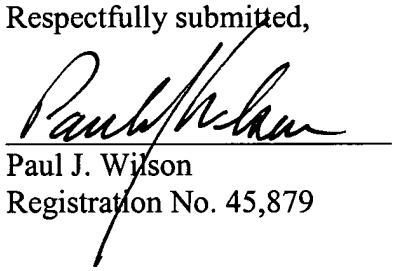
identical to the third impurity region recited in claim 1. *See* page 3 of the June 20, 2003 Office Action. In Porter et al., the n-type impurity region (12) is located in the same area as the active areas, and, in fact, is defined as a source region for the transistor (4). *See* col. 2, line 6 of Porter et al. In contrast, in the present invention, claims 1 and 17 recite a third impurity region that is located away from the active areas. *See, e.g.*, Figure 5, ref. numeral 11; Figure 11, ref. numeral 22; Figure 12, ref. numeral 14 and corresponding text in the instant application. Unlike Porter et al., the third impurity region recited in claims 1 and 17 of the present invention is not part of the active areas of the semiconductor device, and is not located adjacent to active areas of the semiconductor device.

Based on the foregoing reasons, Applicant believes that Porter et al. fail to disclose all of the claimed elements as arranged in independent claims 1 and 17. Therefore, under *Hybritech* and *Richardson*, Porter et al. clearly cannot anticipate the present invention as recited in independent claims 1 and 17. Thus, Applicant believes that claims 1 and 17 are in condition for allowance, and further believe that claims 2-15 and 18-30 are allowable as well, at least by virtue of their dependency from claims 1 and 17, respectively. Applicant respectfully requests that the Examiner withdraw the § 102(e) rejection of claims 1-15 and 17-30.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions and listings of claims in the application:

LISTING OF CLAIMS:

1. (*Currently Amended*) A semiconductor device comprising:

a semiconductor substrate of a first ~~one~~ conductivity type;

shallow trench isolating regions having a first depth, and disposed in surface portions of said semiconductor substrate and defining active areas therebetween;

a first terminal connected to one of said active areas;

a second terminal connected to another of said active areas;

a circuit component connected between said first terminal and said second terminal; and

a protection circuit disposed adjacent to at least said one of said active areas, and comprising:

a first impurity region of said first ~~one~~ conductivity type disposed adjacent to said at least one of said active areas, wherein said first impurity region is a base region of a bipolar transistor,

a second impurity region of a second conductivity type opposite to said first ~~one~~ conductivity type disposed adjacent to said first impurity region, connected to said first terminal, wherein said second impurity region is one of an emitter region or a collector region of said bipolar transistor; and

a third impurity region of said second ~~other~~ conductivity type ~~connected to said second terminal~~, wherein said third impurity region is the other of said emitter region or said

collector region of said bipolar transistor, said third impurity region disposed away from said active areas.

2. (*Previously Presented*) The semiconductor device as set forth in claim 1, wherein said third impurity region further comprises:

a first impurity sub-region disposed in a surface portion of another active area adjacent to said one of said active areas; and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region and extending in said first impurity region under said second impurity region.

3. (*Previously Presented*) The semiconductor device as set forth in claim 2, wherein said first impurity sub-region comprises:

a first portion contiguous to said second impurity sub-region; and

a second portion heavier in dopant concentration than said first portion and connected to said second terminal.

4. (*Currently Amended*) The semiconductor device as set forth in claim 2, wherein said circuit component is a field effect transistor comprising source and drain regions of said second ~~other~~ conductivity type disposed in said one of said active areas, and one of said source and drain regions is said second impurity region.

5. (*Previously Presented*) The semiconductor device as set forth in claim 1, wherein said third impurity region comprises:

a first impurity sub-region disposed in another surface portion of said first impurity region spaced from said second impurity region; and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region and extending in said first impurity region under said second impurity region.

6. (*Previously Presented*) The semiconductor device as set forth in claim 5, wherein said first impurity sub-region comprises:

a first portion contiguous to said second impurity sub-region; and

a second portion heavier in dopant concentration than said first portion and connected to said second terminal.

7. (*Previously Presented*) The semiconductor device as set forth in claim 5, wherein said circuit component is a field effect transistor comprising source and drain regions disposed in said one of said active areas, wherein one of said source and drain regions is said second impurity region, and the other of said source and drain regions is said first impurity sub-region.

8. (*Previously Presented*) The semiconductor device as set forth in claim 1, wherein said third impurity region is disposed in another active area adjacent to said one of said active areas and having a second depth greater than said first depth.

9. (*Previously Presented*) The semiconductor device as set forth in claim 8, wherein said circuit component is a field effect transistor comprising source and drain regions disposed in said one of said active areas, and one of said source and drain regions is said second impurity region.

10. (*Previously Presented*) The semiconductor device as set forth in claim 1, wherein said third impurity region is disposed in another surface portion of said first impurity region and deeper than said second impurity region.

11. (*Previously Presented*) The semiconductor device as set forth in claim 10, wherein said circuit component is a field effect transistor comprising source and drain regions disposed in said one of said active areas, one of said source and drain regions is said second impurity region, and the other of said source and drain region is a part of said third impurity region.

12. (*Previously Presented*) The semiconductor device as set forth in claim 1, wherein said third impurity region extends in said first impurity region under said second impurity region.

13. (*Previously Presented*) The semiconductor device as set forth in claim 10, wherein said circuit component is a field effect transistor comprising source and drain regions disposed in said one of said active areas, and one of said source and drain regions is said second impurity region.

14. (*Previously Presented*) The semiconductor device as set forth in claim 1, wherein said first terminal is a signal output terminal, and said circuit component is an output transistor.

15. (*Previously Presented*) The semiconductor device as set forth in claim 1, wherein said first terminal is a signal input and output terminal, and said circuit component is an output transistor comprising a portion of an input and output circuit connected to said first terminal.

16. (*Withdrawn*)

17. (*Currently Amended*) A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a plurality of active areas disposed in a portion of said semiconductor substrate;

at least one shallow trench isolation region disposed between said active areas;

a first terminal connected to one of said active areas;

a second terminal connected to another of said active areas;

a circuit component connected between said first terminal and said second terminal; and

a protection circuit disposed adjacent to at least said one of said active areas, said protection circuit comprising:

a first impurity region of said first conductivity type disposed adjacent to at least one of said active areas, wherein said first impurity region is a base region of a bipolar transistor,

a second impurity region of a second conductivity type opposite to said first conductivity type disposed in one of said active areas ~~area~~ connected to said first terminal, wherein said second impurity region is one of an emitter region or a collector region of said bipolar transistor; and

a third impurity region of said second conductivity type ~~connected to said second terminal,~~ disposed in another portion of said semiconductor substrate away from said active areas, wherein said third impurity region is the other of said emitter region or said collector region of said bipolar transistor.

18. (*Previously Presented*) The semiconductor device as set forth in claim 17, wherein said circuit component is a field effect transistor.

19. (*Previously Presented*) The semiconductor device as set forth in claim 17, wherein said third impurity region further comprises:

a first impurity sub-region disposed in a surface portion of an active area adjacent to said at least one shallow trench isolation region; and

a second impurity sub-region contiguous to a bottom surface of said first impurity sub-region.

20. (*Currently Amended*) The semiconductor device as set forth in claim 19 ~~18~~, wherein said first impurity sub-region comprises a first portion contiguous to said second impurity sub-region.

21. (*Previously Presented*) The semiconductor device as set forth in claim 20, wherein said first impurity sub-region further comprises a second portion heavier in dopant concentration than said first portion and connected to said second terminal.

22. (*Previously Presented*) The semiconductor device as set forth in claim 17, wherein said at least one shallow trench isolation region has a first depth and said third impurity region has a second depth greater than said first depth.

23. (*Previously Presented*) The semiconductor device as set forth in claim 17, wherein the depth of said third impurity region is deeper than the depth of said second impurity region.

24. (*Previously Presented*) The semiconductor device as set forth in claim 17, wherein said third impurity region extends into said first impurity region under said second impurity region.

25. (*Previously Presented*) The semiconductor device as set forth in claim 17, wherein an upper surface of said third impurity region is contiguous with a bottom surface of said first impurity region.

26. (*Previously Presented*) The semiconductor device as set forth in claim 17, wherein said first impurity region is a p-type impurity region.

27. (*Previously Presented*) The semiconductor device as set forth in claim 17, wherein said second impurity region is a n-type impurity region.

28. (*Previously Presented*) The semiconductor device as set forth in claim 17, wherein said third impurity region is a n-type impurity region.

29. (*Previously Presented*) The semiconductor device as set forth in claim 17, wherein said first terminal is a signal output terminal and said circuit component is an output transistor.

30. (*Previously Presented*) The semiconductor device as set forth in claim 17, wherein said first terminal is a signal input and output terminal, and said circuit component is an output transistor comprising a portion of an input and output circuit connected to said first terminal.